Application manual (Preliminary)

The Pre-Drive PDEC1215A driver

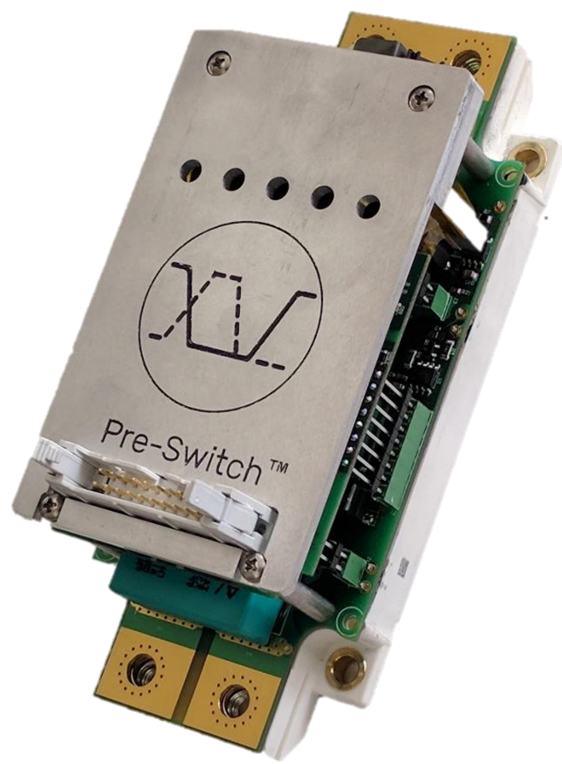
description and application manual

Version 1.1

Abstract

The PDEC1215A is a self-contained, Zero Voltage Switching (ZVS) dual channel half bridge driver made specifically for the Econodual form factor. The driver is based on Pre-switch's Pre-Flex ™ intelligent real time adaptive ZVS architecture, which ensures optimized ZVS switching over a large input voltage, and normal input current range.

Plug and play, the driver interfaces with both the IGBT module and control circuitry like any other driver on the market today, whilst providing 70-80% lower switching losses than hard switching drivers[1]. Additional fault conditions are made available to the user as part of the Pre-Flex 'Blink' protection, and include, industry leading <1us desat protection, OTP for module and driver, OVP and UVP, as well as cycle by cycle current limiting for both IGBT and diode.



[1] Compared to a hard switching driver using sufficient Rg to limit Irr and dv/dt to practical, commercially acceptable levels.

Table of Contents

1. System overview

The Pre-Drive PDEC1215A is the world's first EconoDUAL driver that incorporates built in ZVS circuitry. A plug and play compatible driver, instant benefits include:

1. Lower switching loss for Eon, Eoff and Err, typically 75-80% of total when compared to real world hard switching systems.
2. Higher Fsw for a given current.
3. Higher current for a given Fsw.
4. Lower dv/dt: ~1V/ns turn on, ~2V/ns turn off when Vbus is 800V or below.
5. Reverse recovery overshoot currents <20% of load current.

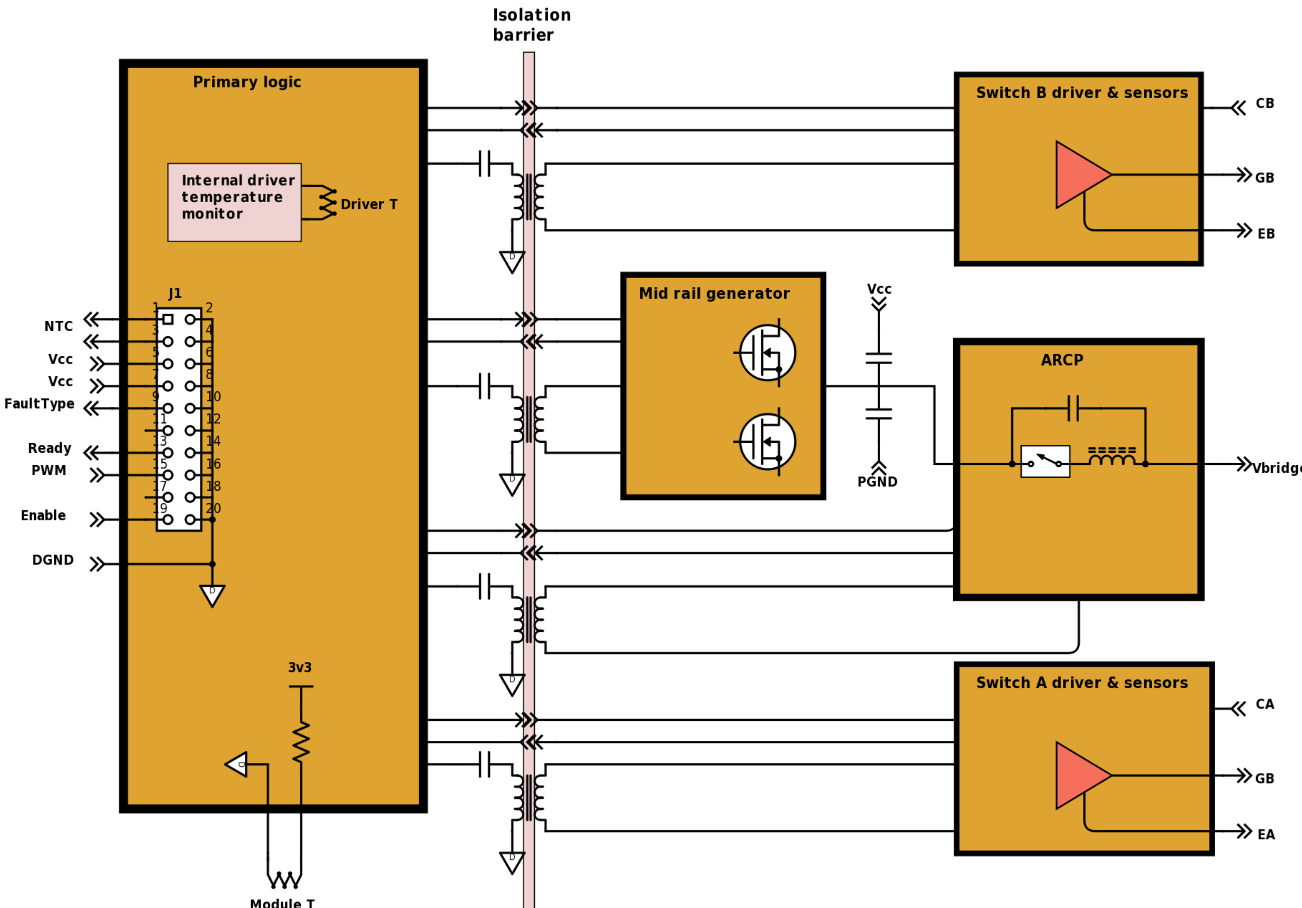


Figure 1: PDEC1215A internal block diagram

2. Operating conditions

2.1 Absolute maximum operating conditions

Parameter	max	unit
Vbus	1100	V
Vcc	16	V
Icc	250	A

2.2 Recommended operating parameters

2.2.1 Voltages

Names	min	typ	max	unit
Vbus	500		800	V
Vcc	14.4	15	15.6	V
Signal Inputs	GND-0.4		Vcc+0.4	V

2.2.2 Currents

Name	min	typ	max	unit
Ibus			220	A
Icc			0.3	A
Ig high		9		A
Ig low		15		A

2.2.3 Fault detection parameters

	min	typ	max	unit
OCP (Vbus = 800)	210	230	250	A
OCP (Vbus = 500)	210	230	250	A
Ibus amps delta per cycle	28			A/cyc
Desat protection	6	7	8	V
UVLO Vcc	12			V
UVLO Vbus	450			
UVLO Vbus hyst		50		V
OVP Vbus			900	V
OVP Vbus Hyst		50		
OTP driver (inductor)			110	Celcius
OTP driver (controller)			98	Celcius
OTP Hyst		14		Celcius

2.2.4 Miscellaneous

	min	typ	max	unit
dv/dt immunity	50			V/ns
V isolation	2500			V
Driver power dissipation		10		W
Fsw	1		20	kHz
Min dead time		1.1		us
Pulse suppression	1			us
Operating T	-40		105	Celcius
Storage T	-40		105	Celcius
Vg high	14	15	16	V
Vg low	-4	-5	-5.5	V

3. Mechanical reference

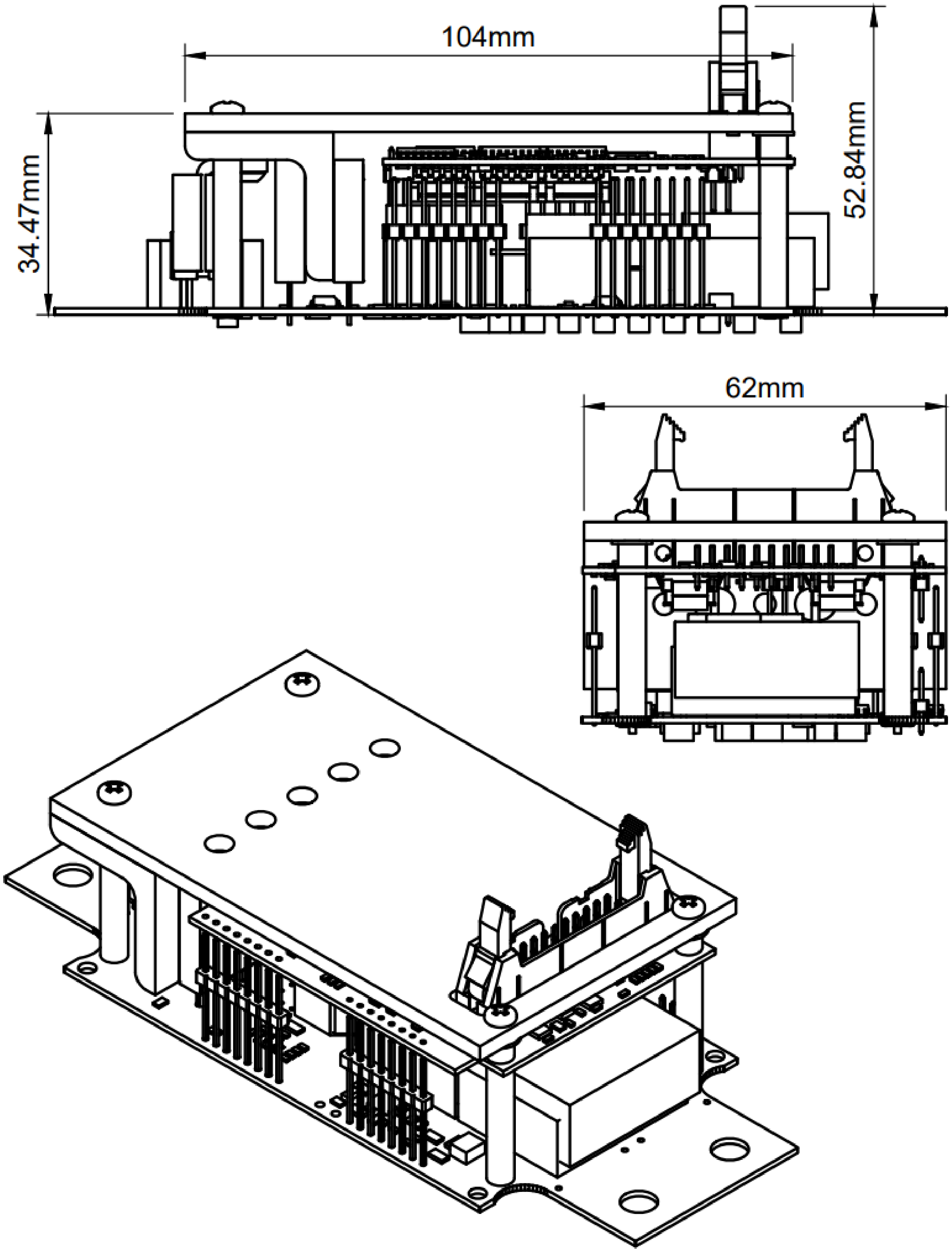


Figure 2: PDEC1215A driver dimensions

4. Assembly procedure

1. Mount driver on module.
2. Screw driver to module at four corners.
3. Solder all pins
4. Screw down power and bridge connections.
5. Connect J1.

5. Interface

5.1 J1 control interface

J1 is the master control interface, and is a standard 10x2 header connection. To ensure against system noise interference, 15V logic is implemented, as well as grounding every even pin.

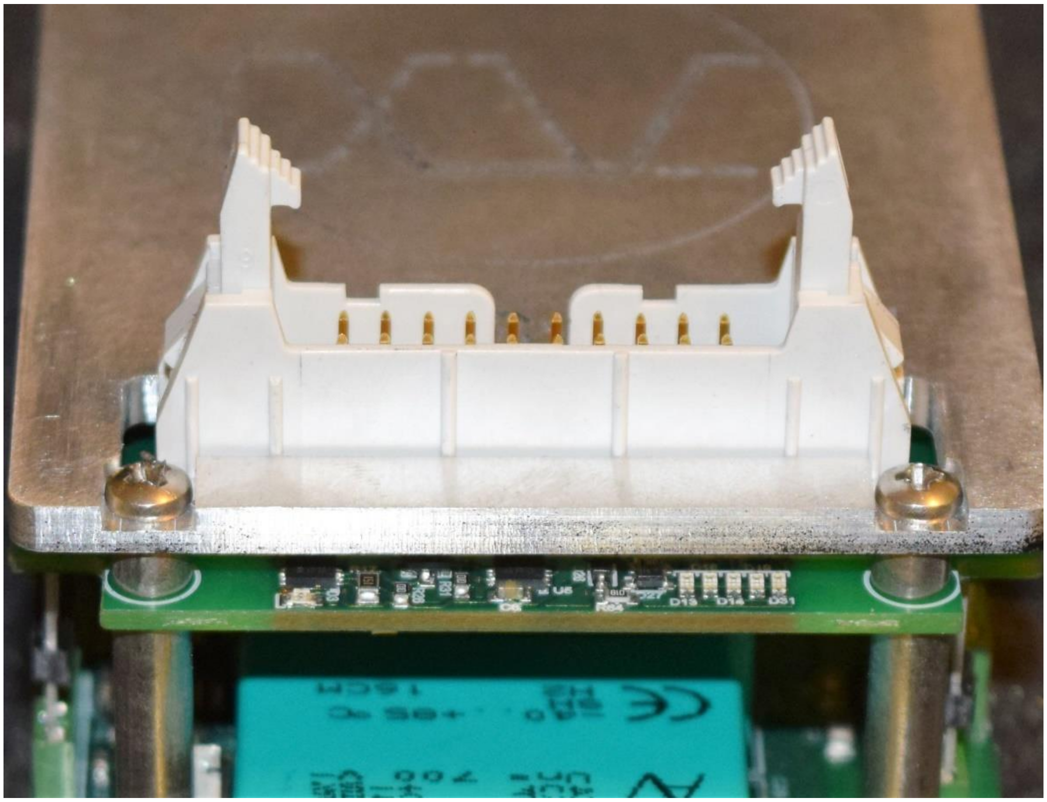


Figure 3: J1 connector

5.2 J1 Pin designation

All even pins are GND

Pin#	name	description	IO
1	NTC	IGBT Module NTC	Pass through
3	NTC	IGBT Module NTC	Pass through
5	Vcc	15V source	Power
7	Vcc	15V source	Power
9	FaultType	Serial debug output	Open drain (internal 27k pullup)
11	UVLO EN	High: Enable the UVLO shutdown feature Low: Allow operation below 500V Vbus	15V CMOS in
13	Ready/Fault	High: Ready, bridge responding to PWM Low: Fault, SwA+SwB disabled	Open drain (internal 27k pullup)
15	PWM	High; SwA off, SwB on, Bridge at +Vbus. Low; SwA on, SwB off, Bridge at -Vbus.	15V CMOS in
17	Data Req	Serial debug enable	15V CMOS in
19	Enable	High; Normal operation. Low; Disable gate drives	15V CMOS in

5.3 Electrical interface

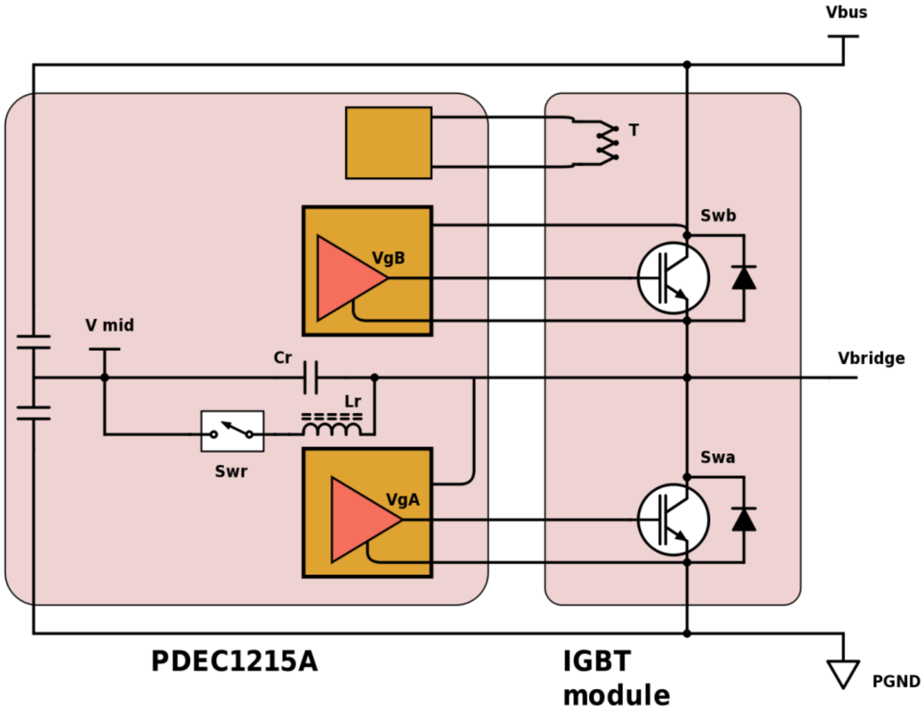


Figure 4: PDEC1215A and IGBT EconoDUAL system interface

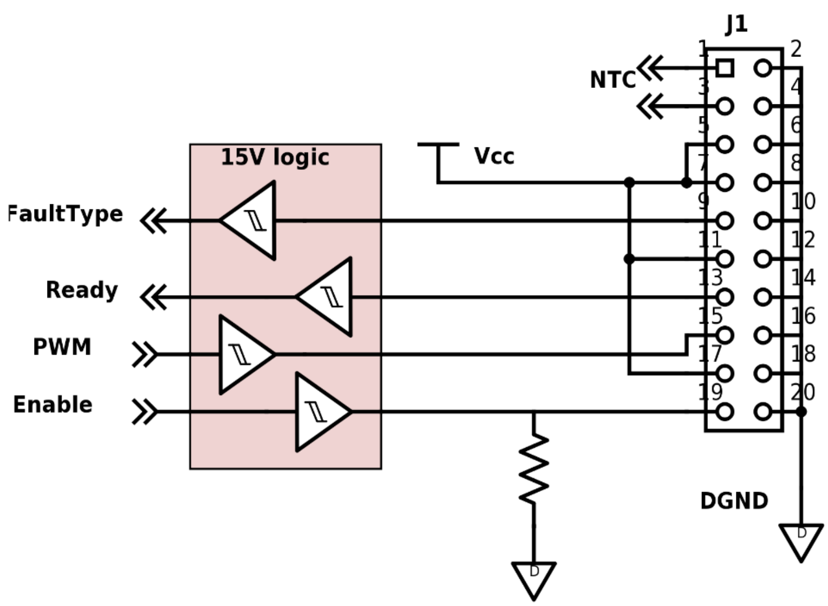


Figure 5: J1 control interface

The recommended logic interface is shown here in Figure 5. All digital IO are 15V logic to improve SNR in industrial environments. The temperature signal and Vref are analogue high impedance signals so buffering is recommended. Vref is provided to allow for higher precision module temperature measurements.

6. LED indicators

Codes are read as big endian when looking at the LED strip at the module power connector end as illustrated in Figure 6: LED indication location below:

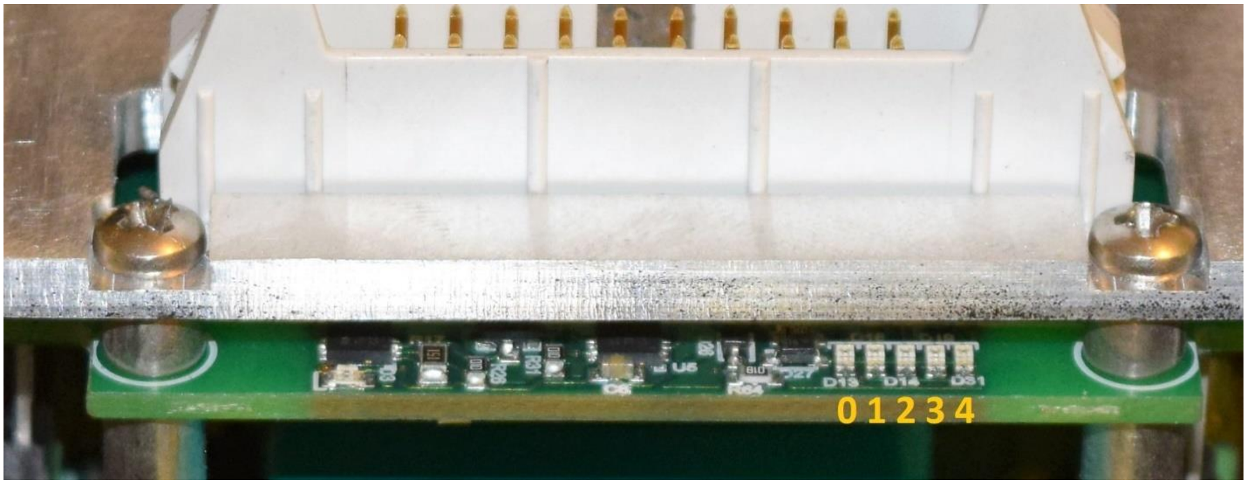


Figure 6: LED indication location and order

7. System operation description

7.1 Normal operation

Under normal conditions, there are 2 possible types of bridge commutation; self, and forced.

Example plots are of a double pulse test comparison running with conditions:

1. Vbus = 800V,
2. Tjv = 100C,
3. Ice = 200A,
4. Device = FF225R12ME4 Infineon EconoDUAL
5. Rg =15.4ohms (Hard switching), (>2.2Ohm soft switching)

7.1.1 Start up

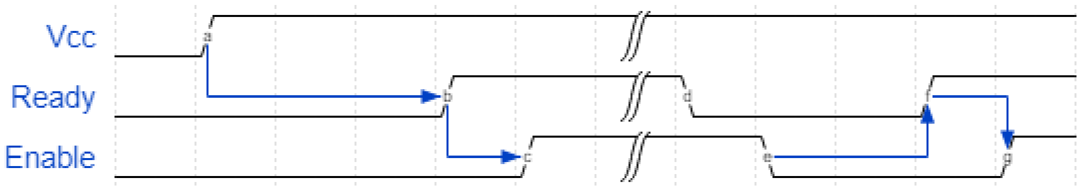


Figure 7: Startup and fault reset sequence

The unit has an internal POR sequence that requires the following start-up procedure:

a) Apply Vcc, J1.19 (Enable) is low
b) Wait for J1.13 (Ready) to go high
c) Set J1.19 (Enable) high to start
d) If J1.13 (Ready) goes low, a fault has occurred.
e) To clear the fault, reset J1.19 (Enable) low
f) Wait for J1.13 (Ready)
g) Set J1.19 (Enable) high to start

7.1.2 IGBT behavior

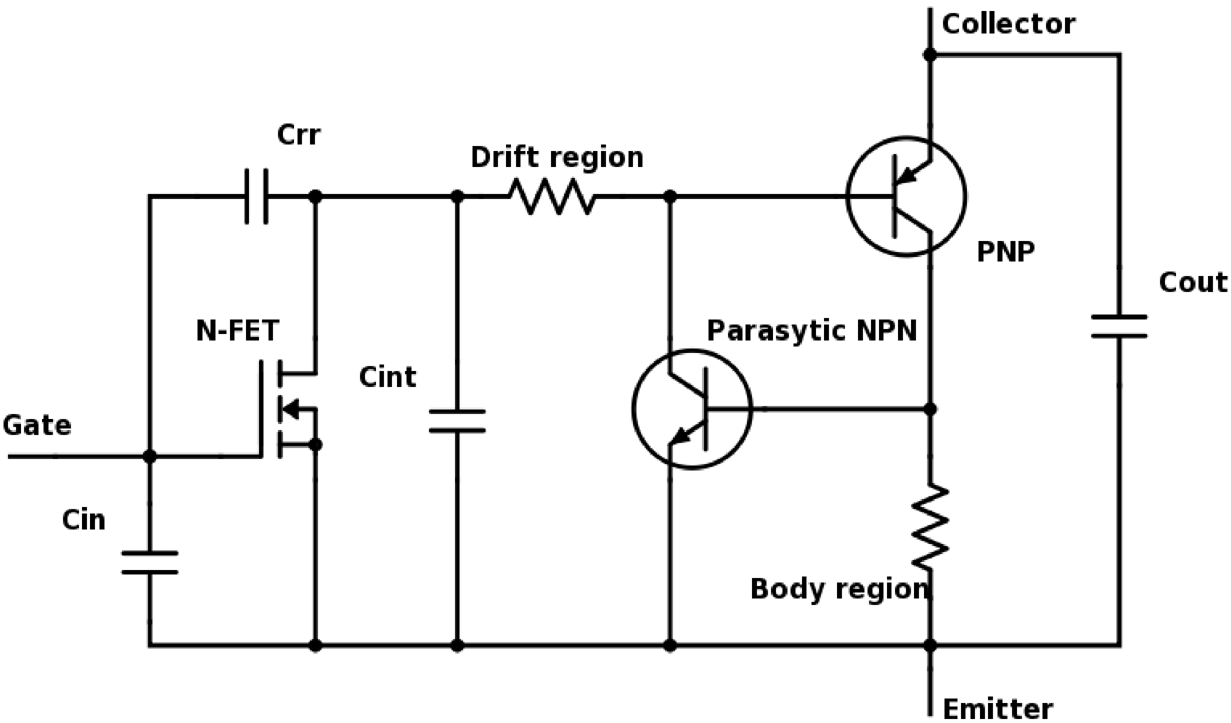


Figure 8: Simplified IGBT equivalent internal circuit

Figure 8 above is a simplified schematic of an IGBT internal componentry, including parasitic effects such as the NPN BJT, responsible for the thyristor effect during excessive body region currents.

7.1.3 Self-commutation

This is the case when the IGBT junction was conducting prior to the commutation, and the device is turned off. The gate voltage is pulled low, which makes the device attempt to turn off. In a normal hard switching scenario, the device Vce will begin to climb, which will then inject charge to the gate via the reverse capacitance Cr (insert schematic). This biases the gate back on, holding the IGBT in linear mode until the Vce reaches Vbus. Current through the device remains fairly constant until this time, the result is large Eoff losses as illustrated in Figure 9 below. Figure 10, in contrast, shows the effect of adding substantial capacitance across the bridge node to the rails. This time as the IGBT attempts to turn off, a large portion of the current is diverted to the parallel capacitance. The result is not only a substantial reduction of Eoff, but also a dramatic reduction of rising edge dv/dt.

In the examples provided, the ZVS turn off current reduction isn't greater in part due to the type and generation of IGBT of the Infineon module. The IGBT's internal BJT junction continues to conduct current proportional to the base current scaled by the BJT beta value, as the internal N-FET output capacitance (Cint in Figure 8 above) fills with rising Vce. A much lower Cint, or lower BJT beta, would make Crr the dominant feedback path, and would result in a larger Eoff reduction.

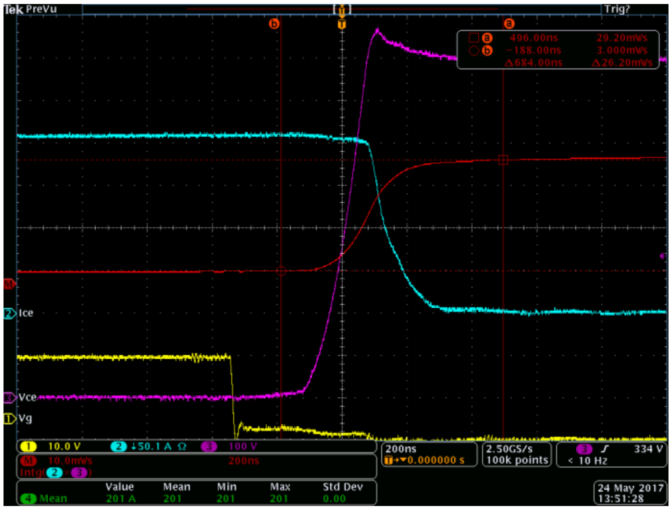


Figure 9: Hard switching turn off

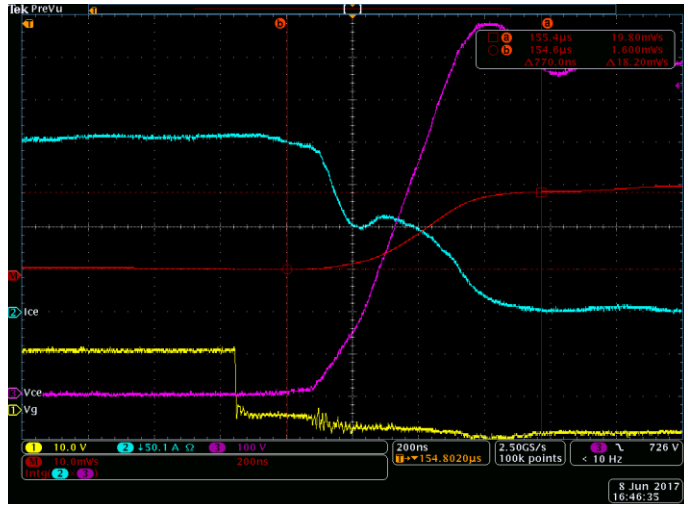


Figure 10: Low loss turn off (ZVS)

7.1.4 Forced-commutation

In this instance, the IGBT in question is off, and the anti-parallel diode is conducting. In this condition, simply turning off the opposing IGBT will have no effect as it was not conducting as stated. To commutate in this state, an external current must not only remove the current from the conducting diode, but also have additional current to discharge the bridge capacitance.

To limit stress conditions such as diode reverse recovery current (Irr) spikes and high dv/dt Vbridge transitions, hard switching systems select a gate drive resistance Rg such that turn on speed is limited. This restricts the di/dt experienced by the diode conducting prior to Vbridge commutation, which results in a greatly reduced Irr, and therefore lower peak current through the turning on IGBT. As the voltage across the IGBT falls, the parasitic reverse capacitance (Crr) biases the IGBT's internal MOSFET into linear mode. This ensures a more controlled and gradual voltage rise, at the expense of increased Eon loss energy.

To what degree these parameters vary depends heavily on the IGBT generation, manufacturer, temperature, tolerances, and of course operating volts and current. The system designer must take this into account- normally. As the PDEC1215A includes internal ARCP, parameters such as di/dt and dv/dt are not controlled by Rg, which is therefore set to the minimal resistance practical to ensure minimal loss.

Comparing the two approaches, Figure 11 below illustrates the transition behavior of a hard-switching driver with test conditions outlined above. The red trace indicates the energy lost (mWs = mj) due to the product of the IGBT current and voltage. A slowed dv/dt and reduced Irr come at the cost of increase switching losses.

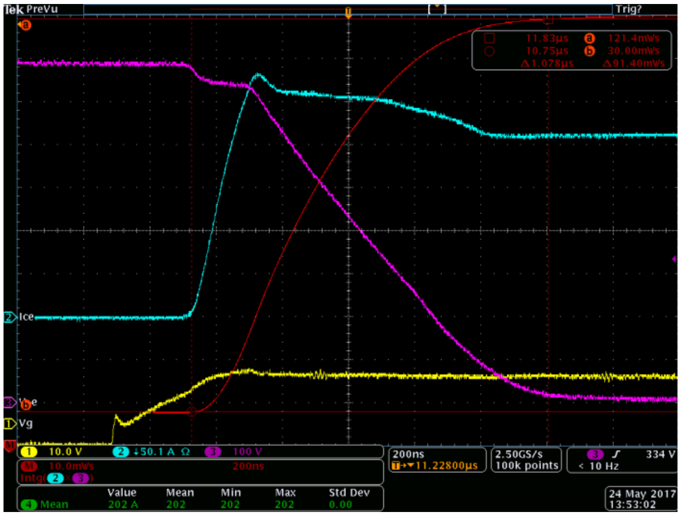


Figure 11: Hard switching turn on

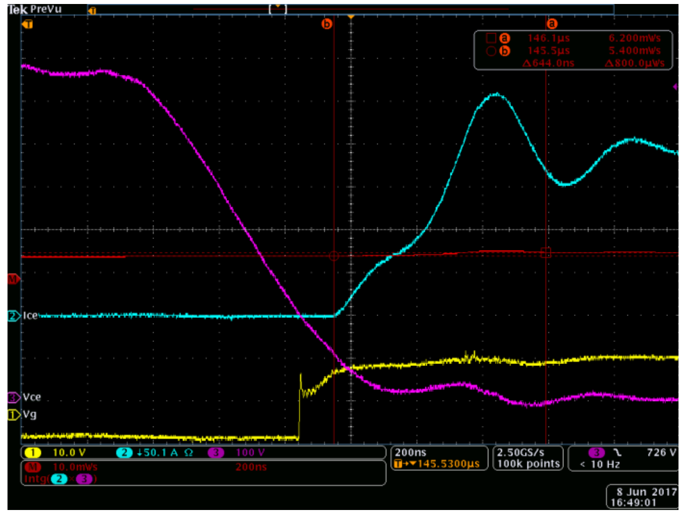


Figure 12: Low loss turn on (ZVS)

Conversely Figure 12 shows that further improved reduction in dv/dt and Irr can be achieved while virtually no loss when using a correctly timed ARCP system.

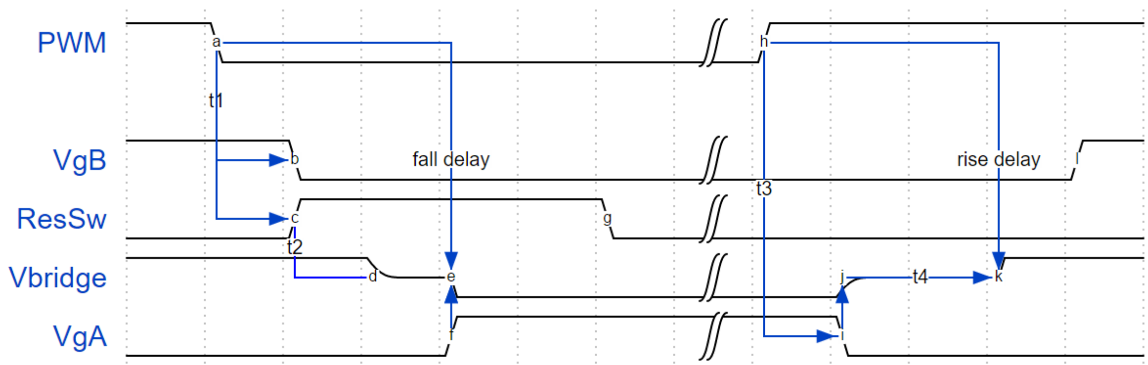


Figure 13: Forced and self-resonance transition

Referring to Figure 13 above, the forced-resonance sequence of events is as follows:

a) The controller initiates a state change by transitioning PWM from high to low, which will ultimately change the bridge voltage from Vbus to ground.
b) After a short delay t1, VgB, the gate voltage of the top IGBT will fall. Note that when a forced resonant transition is happening, the diode is conducting, and not the IGBT.
c) The ResSw or resonant switch turns on the ARCP, charging the resonant inductor, and reducing the conducting diode's current to zero.
d) Once the resonant circuit current exceeds the load current (and any additional diode Irr), the Vbridge will begin to fall.
e) The Pre-Drive controller detects when Vbridge reaches a minima, which will generally be very close to rail, which is ground in this example.
f) The low side IGBT VgA is turned on to coincide with Vbridge minima to ensure optimal ZVS switching.
g) ResSw continues conducting until the resonant current is discharged.

The self-resonance sequence of events is as follows:

h) The controller initiates a state change by transitioning PWM from low to high, which will ultimately change the bridge voltage from ground to Vbus.
i) After a short delay t4 the low side IGBT is turned off via VgA.
j) Vbridge starts to rise gradually as the load current fills the external resonant capacitors.
k) The high side diode begins to conduct as Vbridge reaches Vbus.
l) The high side IGBT is turned on via VgB

7.2 *Fault conditions (Blink)*

In the event the sensed parameter exceeding those specified in section 0, the following sections specify the resulting driver behavior.

In a system shutdown, the IGBT gates and mid-rail generator are disabled simultaneously. the IGBT Vce will rise with acceptable dv/dt due to external parallel resonant capacitance. If fault occurs during a state transition, the transition is completed first.

7.2.1 Fault codes

*Any codes not listed are reserved.

Fault	LED code	Reaction time	System reaction
None	0x00	NA	NA
Internal Error	0x01	<1us	System shutdown. Restart must be initiated by master controller by toggling ‘Enable’.
Desat	0x02	<100us	System shutdown, system will self-enable once Vbus falls below Vmax – (Vbus hyst).
OCP	0x03		
Vbus UVP	0x04	<100us	System shutdown, system will self-enable once Vbus rises above Vmin + (Vbus hyst).
Vbus OVP	0x05	3 cycles	System shutdown. Restart must be initiated by master controller by toggling ‘Enable’.
Vcc UVP	0x06	<1ms	System shutdown, system will self-enable once Vcc rises above Vcc min.
Module OTP	0x07	<1ms	System shutdown, system will self-enable once module temperature falls below module OTP – (OTP hyst).
Driver OTP	0x08	<1ms	System shutdown, system will self-enable once module temperature falls below driver OTP – (OTP hyst).
Multiple error	0x09-0x0C		

7.3 Serial output protocol

A unidirectional serial interface provides feedback to the controller indicating the source of any existing faults and the latest ADC measurement of the VDC bus.

Upon assertion of the “Data Req” pin, the following 4-byte packet structure is transmitted:

Synch frame (0x55)	Reg0: Error byte	Reg1: VDC ADC byte 1	Reg2: VDC ADC byte 2

Transmission continues until the “Data Req” pin is low.

The asynchronous serial byte format is as follows:

SB	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	SP

SB: Start bit, LOW
bit 0 - bit 7: Data Byte (non-inverted)
SP: Stop bit, HIGH
Transmission rate: 115,200bps
The individual byte formats are as follows:

7.3.1 Reg0, Error Byte

Bit	Label	Description
0	Gate Fault	0 = gate drive normal, 1 = gate drive error detected
1	OCP	0 = bridge current normal, 1 = bridge over current detected
2	Desat	0 = normal, 1 = desat event detected
3	Source of fault,	0 = Low Side, 1 = High Side
4	OVLO/UVLO fault,	0 = VDC within operating range, 1 = VDC outside of range
5	VCC fault,	0 = VCC above VCCmin, 1 = VCC above VCCmin
6	Driver over temperature,	0 = driver below TDmax, 1=driver above TDmax
7	Module over temperature,	0 = module below TMmax, 1=module above TMmax

Note, Error source bits 0-3 cause a fault to register until the reset input is toggled. The value of Reg1 is held until the reset pin is pulled low.
Error source bits 4-7 will put the module in a fault state only while the fault condition is met. These values are not cached.

7.3.2 Reg1, Vcc ADC byte 1

Bit	Label	Description
0	OVLO	0 = VDC lower than VDCmax, 1 = VDC higher than VDCmax
1	UVLO	0 = VDC higher than VDCmin, 1 = VDC lower than VDCmin
2	always zero	
3	always zero	
4	ADC result bit 0	
5	ADC result bit 1	
6	ADC result bit 2	
7	ADC result bit 3	

7.3.3 Reg2, Vcc ADC byte 2

Bit	Label	Description
0	ADC result bit 4	
1	ADC result bit 5	
2	ADC result bit 6	
3	ADC result bit 7	
4	ADC result bit 8	
5	ADC result bit 9	
6	ADC result bit 10	
7	ADC result bit 11	

7.3.4 Desaturation (desat)

As with traditional Econodual drivers, the PDEC1215A is equipped with IGBT desaturation detection and protection. When a given IGBT is 'on', its Vce level is monitored. Should Vce exceed the value specified in section 2.2.1, the IGBT is turned off, and the system raises an error to the controller. Cr in Figure 4 ensures a reduced Vbridge dv/dt and overshoot voltage under these conditions.

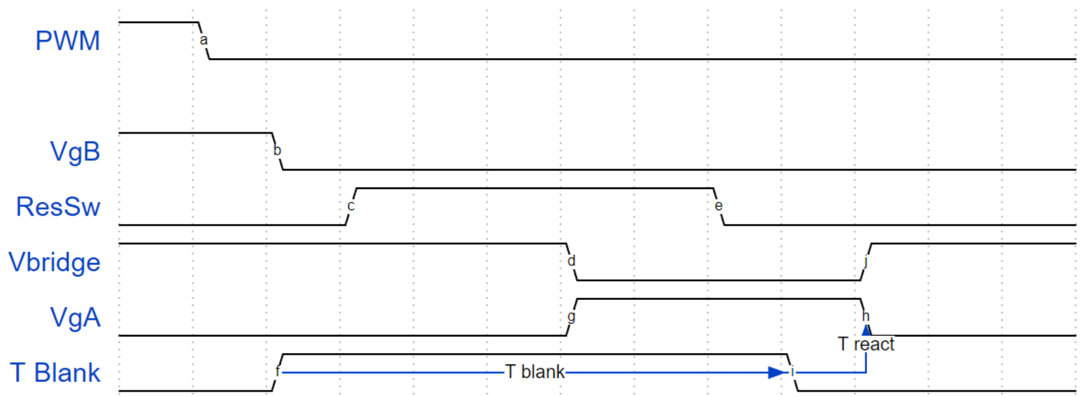


Figure 14: Ton desat event response

Figure 14 shows T blank for the 'on' transition. As can be seen, the blanking period must wait for the resonant transition and turning on IGBT settling time.

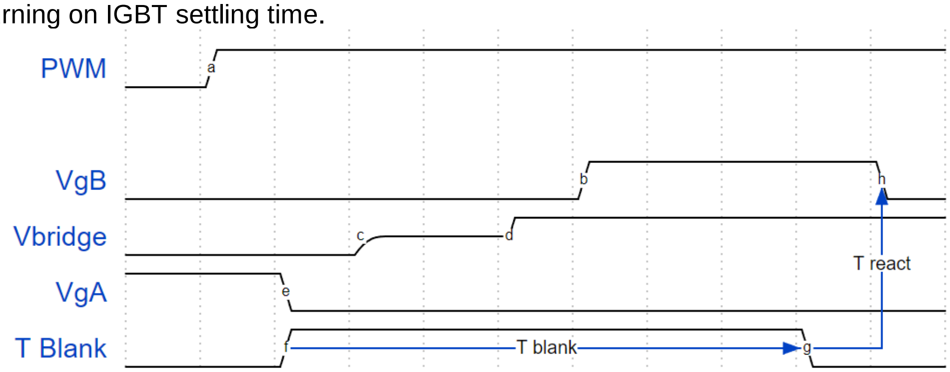


Figure 15: Ton desat event response

Toff desat dely is shown above in Figure 15. As this is the self-resonant edge, T blank is purely a function of the dead time and the turn on settle time. The unit can be restarted by toggling the Enable line.

7.3.5 Vbus Over Voltage, Under Voltage Protection (OVP, UVP)

To be able to perform ZVS switching within bounded timing constraints, Vbus must be of a minimum value. Over voltage can cause excessive Vce levels across the IGBTs during turn off. Therefore the PDEC1215A monitors Vbus continuously, raising a fault to the controller if Vbus goes out of bounds. To prevent oscillations, the system uses hysteresis to ensure Vbus recovers sufficiently before clearing the fault.

7.3.6 Over Current Protection (OCP)

Due to the current tracking capability unique to Pre-Drive technology, the PDEC1215A is able to sense when current is outside levels listed in section 2.2.2. This differs from 'desat' protection in the following key ways:

1. Detection only occurs during forced commutation.
2. Sensed current is based on the known parameter Lr, and on measured parameters Vbus and time t2 (Figure 13) using equation:

$$Ice = \frac{Vbus * t2}{Lr} \tag{1}$$

This requires that the system Fsw is great enough such that the load current variation occurs at or below the maximum amps/transition ratio specified in section 0. Requiring 3 cycles to confirm an over current event, the current sensed is not subject to IGBT temperature or generation type such as desat does, and is therefore more accurate.

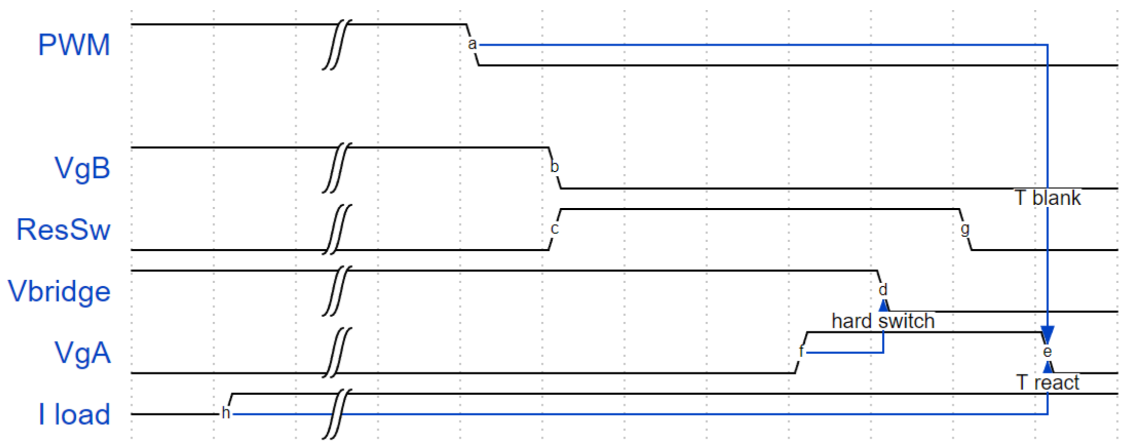


Figure 16: OCP worst caseresponse timing delay

Figure 16 shows the worst case OCP detection timing. As current below desat levels is only assessed during transition, the system cannot react until the next transition to follow the over current event. The unit can be restarted by toggling the Enable line.

7.3.7 Vcc UVP

Both the primary and all secondary controller sections include system UVP. On the primary side, Vcc is monitored. The isolation transformers will not switch until Vcc reaches the minimum voltage specified in section 2.2.1. Each secondary side subsystem also has its own internal UVP to prevent any dangerous partial operation. When Vcc and all other internal voltages rise above minimum levels, normal operation will commence.

7.3.8 Module/driver Over Temperature Protection (OTP)

The driver has 2 internal thermal sensors to ensure safe operation within specified environment conditions. See Figure 17 for details. In the event of an over temperature condition, the device will shut off and indicate the corresponding error code listed in section 7.2.1. The unit can be restarted by toggling the Enable line once the unit has cooled sufficiently as per section 2.2.3, Fault detection parameters.

8. Safe operating area

The PDEC1215A has 2 internal temperature sensors that will protect the driver operating within the operating conditions specified below. Note this assumes an ambient of no greater than 50C. Note that the unit can handle higher operating points if sufficient forced air is available.

Figure 17 below show the safe operating area with minimal airflow which would be expected in an environment with passive convection, and assumes an ambient <50C.With no airflow, the unit will likely shut off with showing thermal error codes. For DC, operate the device at the equivalent Irms value for a given Fsw and Vbus.

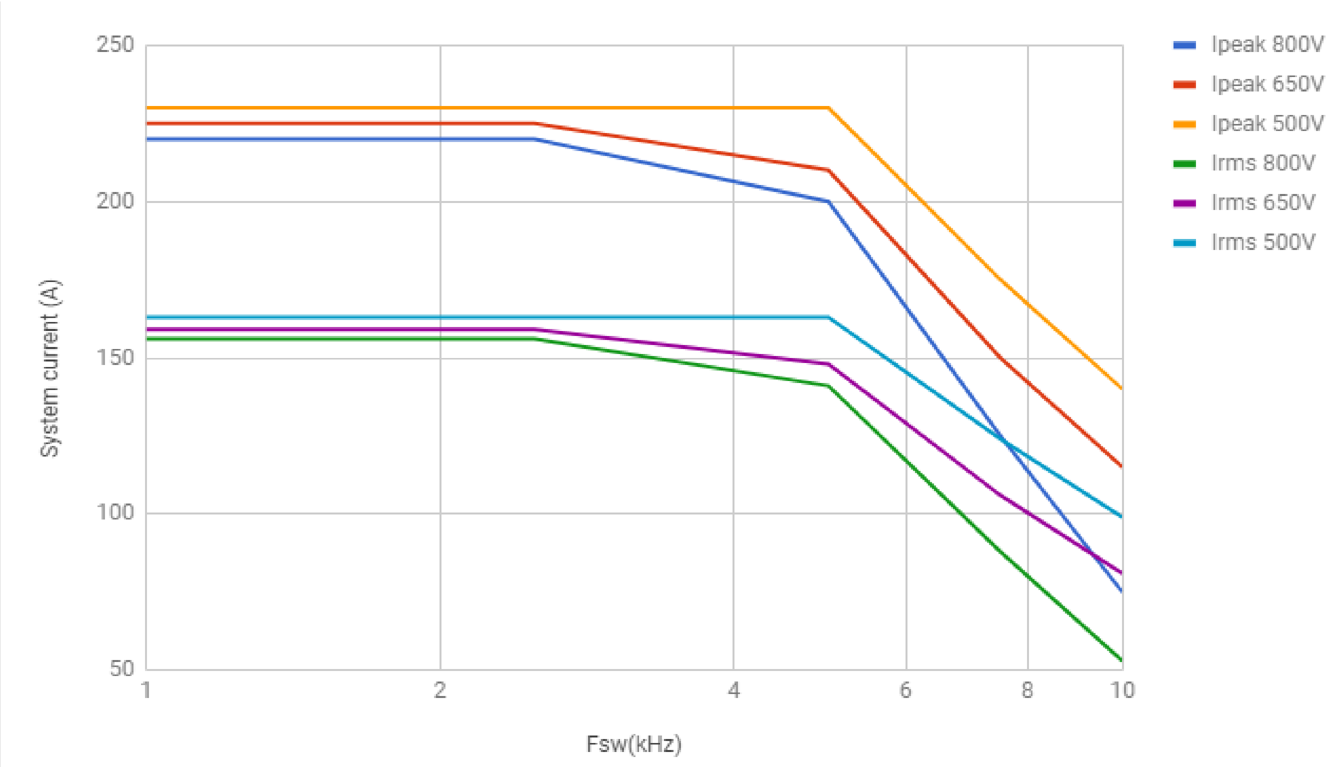


Figure 17: Safe operating area for a 60Hz sine wave

9. Bibliography & recommended reading

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10. Ordering and Technical support

Please visit https://www.pre-switch.com for ordering information.

11. Legal disclaimer

The PDEC1215A is intended purely to demonstrate Pre-Flex's ZVS controller capability, and is not intended for any application other than feature and performance assessment. Only a qualified and experienced user should operate this device. Pre-Flex accepts no liability for injury or property damage due to use of this device or supporting documentation.

Appendix A. Definitions, Acronyms, and Abbreviations

ARCP	Auxiliary Resonant Commutated Pole
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
OVP	Over Voltage Protection
UVP	Under Voltage Protection
OTP	Over Temperature Protection
Desat	Desaturation